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Implementation of Clock Gating Method to Reduce Power Dissipation for Red Channel Equation

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Abstract**—***Due to the exponential decay that light experiences during its journey, underwater photographs often have low contrast and color distortion. Additionally, the attenuation rates of colors associated with different wavelengths vary, with red being the wavelength that attenuates most quickly. A technique called red channel compensation was proposed to repair underwater photos, in which colors associated with short wavelengths are retrieved as would be expected for underwater images, restoring the lost contrast. In this paper the low power pipelined architecture with clock gating is implemented and verified for its functionality and power reduction.*

Keywords- *Architecture Design, Red Channel Compensation, Underwater Image Processing, Red Channel equation, Clock gating technique, DAG.*

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I. INTRODUCTION

Exploring marine resources requires the use of the video captured by underwater imaging technology, which is abundant in the ocean. More and more underwater robot technology is being used now than ever before. A lot of undersea data is needed for submarine tourism, underwater facility maintenance, and resource research. Because of the unique optical conditions in the ocean, captured data is more likely to experience quality issues such as color shift, edge blur, and contrast decrease. Degraded photographs are quite problematic for later research projects as a result, underwater imaging has drawn considerable attention, and numerous academics have conducted extensive research.

In [2], The two main kinds of underwater picture enhancement techniques used today are: (1) those based on conventional underwater image enhancement algorithms like the histogram equation, wavelet transform, sharpening, and Retinex, etc. and also authors proposed an underwater picture improvement algorithm that stretched the image's RGB and HSI color gamuts consecutively using an integrated color model (ICM) based on sliding histogram. However, the algorithm's parameters must be manually modified to match the supplied image.

This work suggests a straightforward and efficient underwater picture restoration approach based on the attenuation characteristics of various wavelengths to address the image distortion produced by the red component attenuation. The intensity information and attenuation traits of various channels are analyzed to create a red

channel weighted compensation model and the edge data of the compensated red channel is refined via guided. filtering. The gamma correction model is used to increase contrast in order to clear up photographs.

In [3-5] Power consumption is currently a significant barrier to the performance of VLSI designs. The main causes of the restricting technology developments are technological restrictions and requirement constraints. Power dissipations for a silicon device have two parts: a static component and a dynamic component. To decrease overall power dissipation, both of these components must be decreased. Static power is created by the leakage current that a transistor produces. Dynamic power, on the other hand, is due to switching of the transistor from one logic value to another. Since dynamic power depends linearly on frequency, power dissipation can be minimized by using a clock gating method for red channel compensation block proposed in [2]. The rest of the paper is organized as follows. Section II discusses about the red compensation block. Section III discusses about introduction of clock gating into the equation in order to reduce power consumption. Section IV discusses the results of simulation and synthesis carried out for the architecture and Section V concludes the work.

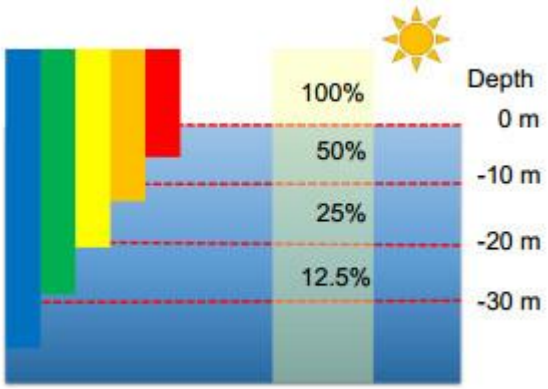

Fig1- Light absorption at different wavelengths underwater.

II. COLOUR COMPENSATION IN UNDERWATER IMAGES

Existing work uses approaches from wavelength correction and image de-hazing (WCID) to reduce distortions in light scattering and gradation. To estimate the distance of objects in the scene to the camera, the dark channel prior to the existing scene depth source approach is utilized initially. The low intensity in the dark channel is primarily determined by three variables.

1) shadows in photos of the seabed, those are casted by the items such as, zooplankton, seaweeds, or rocks.
2) Specific color channels are absent on colored surfaces such as blue flora, red or yellow sand, and colored minerals.
3) Foreground and background photos are segmented into dark ecosystems or surfaces depending on the depth map.

The blue tones are subsequently corrected by doing energy compensation on each color channel. The PA (Planar Assumption) technique uses image enhancement to enhance the image quality of underwater photographs. Expensive optical gear or numerous pairs of stereo pictures are no longer required with WCID. WCID enhances visibility while also assisting in the restoration of underwater picture color balance, leading enhanced image clarity and great colored fidelity.

A. Module

• Segmenting the foreground and backdrop
• Use colour enhancement in contrast.
• Determine the MSE and PSNR.
• PA is making adjustments for the light.
• There is scattering and a shift in hue.

B. Fog Modeling

•The higher particles in the photograph are fog, which is created by water droplets.
• The effect is a colour change in the context of an underwater photograph.
• The Proposed task is to improve the image quality and to improve the PSNR and MSE by employing PA.
• PA is used to locate the haze and eliminate its effects; this procedure is more effective than WCID.
• For the underwater shots, each of these pictures was taken using a light source.

BLOCK DIAGRAM

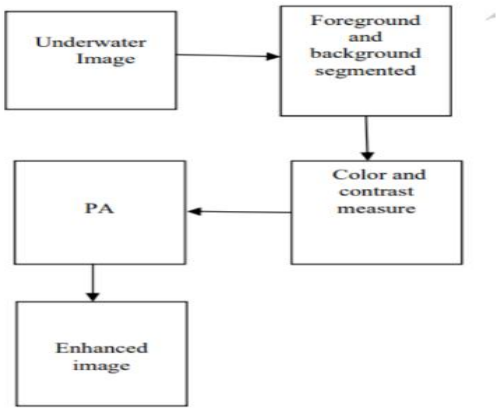

Fig2– Block diagram for color compensation

III. POWER REDUCTION USING CLOCK GATING TECHNIQUE

Power optimization is required due to the ever-rising number of transistors installed on a chip. The potential for energy optimization is growing right now as technologies like smart grids are created. A "smart grid" is an electrical system that incorporates fundamental components, such as sensor and controller systems, that may be implemented as silicon on chip (SOC) integrated circuits at very large scales (VLSI). Both sequential and combinational circuits are used in VLSI. The clock is the primary source of dynamic power consumption in sequential circuits. By reducing idle clock cycles, the clock gate approach lowers the clock's power usage.

Depending on the application, how much power the circuit must dissipate is one of the important requirements in the design process. Any circuit's overall power consumption consists of both static and dynamic power. Reducing the power conversion that occurs in the clock network and the switching operation brought on by the elements kept in the clock's idle state will both result in energy savings. 70 to 90% of the dissipated power is made up of the converted power. Switching activities can be utilized to find average power usage, hence helping to analysis speed performance.

Three different cell types use the clock gating technique:
1) Latch based cell
2) Flip flop-based cell
3) Gate based cell

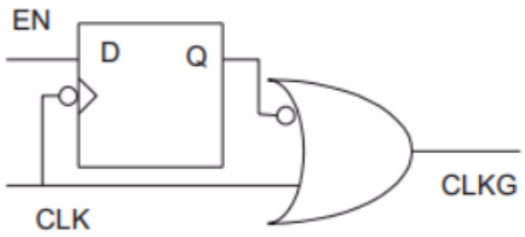

Fig3 -A CG using D flip flop, negative edge triggered along with OR gate.

• Module-level CG
• Register-level CG
• Cell-level CG

Module-Level CG: This level of control allows for significant power savings by turning off an entire block or module in the design. The clock to a single register or a group of registers is gated in the Register-Level. Cell-Level Gating: By including a CG circuit as a component of the cell, the cell designer introduces a cell-level CG and relieves the circuits' burden.

IV. PROPOSED CLOCK GATING ARCHITECTURE

The problem of restoring degraded images from the underwater environment is challenging, in part because light traveling underwater is subject to two combined attenuations, called scattering and absorption. The first is the change in direction of light upon impact with particles, and the second explains how light is absorbed by particles.

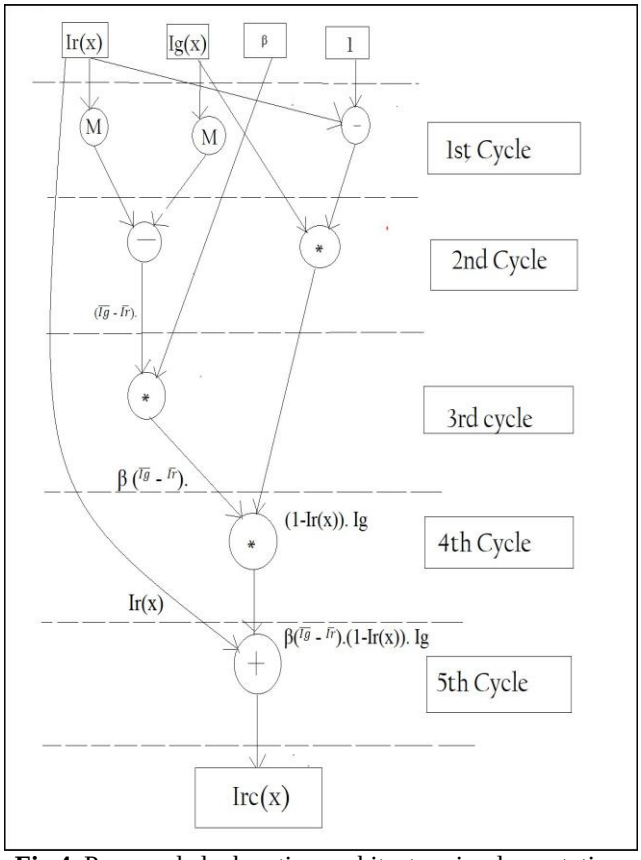

Fig.4. Proposed clock gating architecture implementation.

The final image has a distinctive bluish hue because of shorter wavelengths (green - blue) give the scene deeper insight than the longer wavelengths (red), which are fast disappearing. together. As the performance overall of the algorithms is greatly reliant on environmental factors, this presents a challenging recovery challenge in addition to the turbidity of the water and other organic suspended particles in the medium. In order to try to broaden the range of what may be seen in the scene, an artificial source of light is normally added to the imaging device.

In images captured underwater, since the red channel is the fastest to attenuate, the informational content of the red channel is almost lost. To compensate for this red channel loss, an efficient red compensation block can be used to overcome this loss so that the mathematical equation can be expressed:

Irc(x)=Ir(x)+β ($\bar{\bar{Ig}}$ - $\bar{Ir}$). (1-Ir(x)).Ig

Ir(x)=Red-coloured intensity value set

Ig(x)= green-coloured intensity value set

$\bar{\bar{Ig}}$= mean value of green coloured intensity values

$\bar{Ir}$= mean value of red coloured intensity values

Directed Acyclic Graph (DAG): An directed graph is a directed graph with out any directed cycles in mathematics, particularly graph theory. That is, it is made up of edges and vertices with each edge travelling from vertex to vertex, hence travelling in all of these directions will never result in a closed loop. A directed graph is a DAG if and only when its vertices can be arranged topologically in a linear way that matches all edge directions.

Once the DAG is computed then different low power techniques like clock gating, power gating, pipelining, parallelism and etc can be added in order to reduce power dissipation.

The clock signal is removed from the circuit when it is not in use via the clock gate approach, which is utilized in several synchronous circuits to minimize power dissipation. The clock gating method increases the amount of

logic in a circuit at the expense of energy savings by reducing the clock tree. utilizing the 45nm cadence tool, and is compared to the real design in Fig. 4. The clocking cycle for every phase is represented in this design by all dotted lines. Clock gates may be used in phase 3 of this architecture, as can be seen by looking at it. Therefore, the stage 2 clock gate is implemented in the operation of the multiplier to reduce the power dissipation during one clock cycle. Once a stage 3 multiplier operation is complete, the clock gate is enabled for stage 4 operation. Each stage uses one clock cycle for its processing. The average of the color planes (μ) was pre-calculated and provided directly as input to step 1 for the processing of underwater images.

IV. EXPERIMENTALRESULTS

The proposed hardware design flow was Verilog code and simulated using Cadence Sim Vision tool. The Fig.5 shows the synthesized hardware of proposed architecture. The Synthesis was done using Cadence Genus tool for 45nm technology node.

Fig.6. shows the simulation output before implementing the clock gating.Fig.7. shows the synthesized hardware of proposed architecture for clock gating model. The Synthesis was done using Cadence Genus tool for 45nm technology node

Fig.8. shows the simulation output after implementing the clock gating. The images obtained with both hardware and software simulations are qualitatively similar. Hence, the proposed hardware design is efficient in red channel compensation.

From the below simulation results the power dissipation will be more before clock gating. Fig.7. shows the clock gating that is been introduced in the circuit Fig.8. shows that after clock gating for one cycle power dissipation might get reduced after applying clock gating. Since extra AND circuit is introduced in the architecture, there might be a slight increase in the area. Therefore, by applying clock gating speed of computing will be faster.

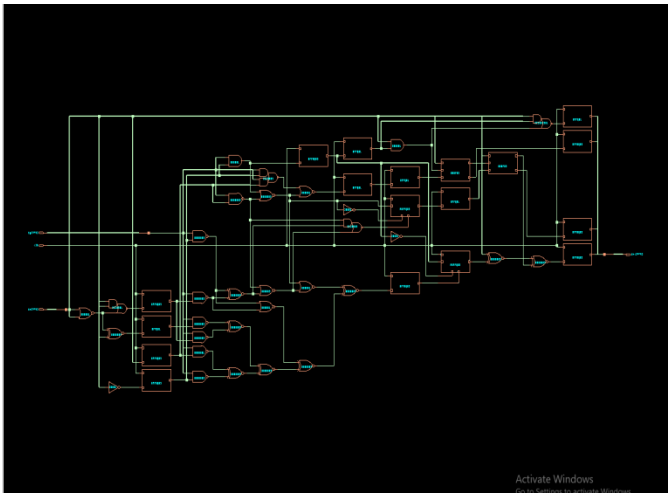

Fig.5. Synthesized circuit for proposed hardware design for red compensation block.

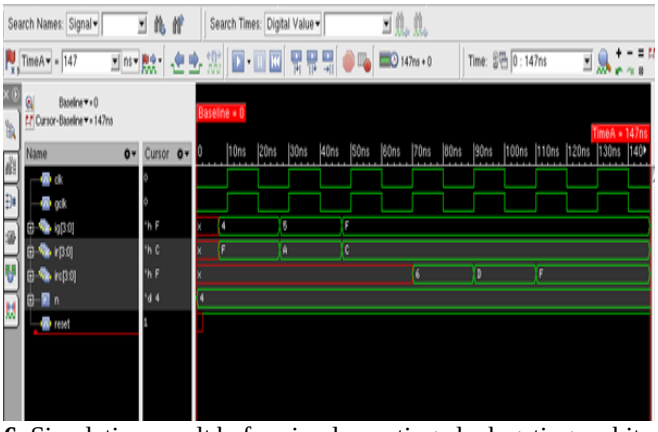

Fig . 6. Simulation result before implementing clock gating architecture.

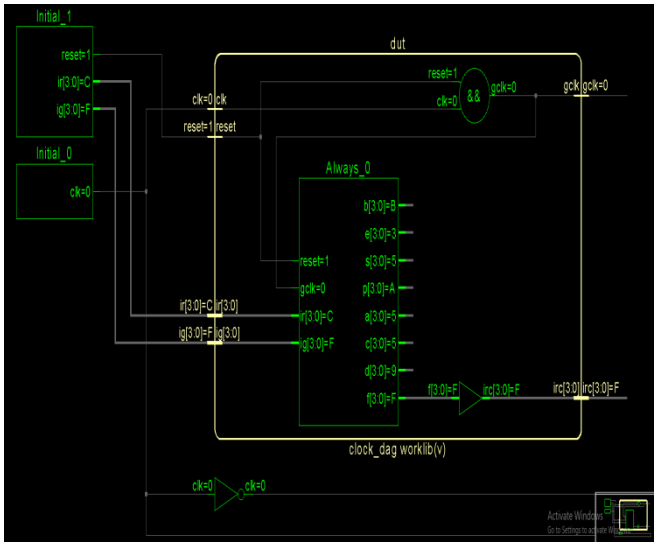

Fig.7.Synthesized circuit for proposed hardware design for clock gating block

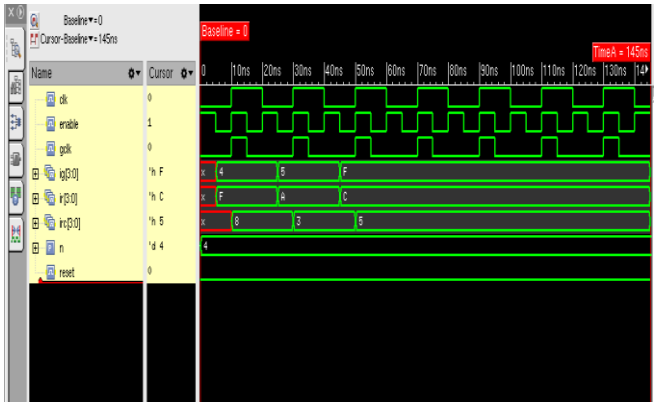

Fig. 8. Simulation output of after implementing clock gating

The Fig 5 shows the hard ware design for the proposed work of red channel compensation using the clock gating technique. The respective simulated output is obtained as shown in the Fig 6 here we observe the clock latency up to 70nsec it is the time taken to compute all the 5 cycle shown in Fig 4 architecture implementation. Fig 7 shows the hard ware implementation of the clock gating technique block by which the overall clock latency is reduced to 10nsec shown in Fig 8. The Table 1 shows the comparisons of power dissipation between the with clock gating technique and without clock gating technique, by which the total power of with clock gating is less when compared to without clock gating technique.

Table.1 Comparisons of Power Dissipation

Design	Leakage Power (nW)	Internal Power (µW)	Switching Power (µW)	Total Power (µW)
Without clock gating	2.956	2.125	0.2686	2.396
With clock gating	2.732	1.835	0.2458	2.083

V. CONCLUSION

In this paper, clock gating architecture is been implemented for red channel compensation which is an essential block in underwater image processing in order to resolve the red artifacts that appear in the enhanced under water images. The advantage of having such hardware design is to improve the performance of the algorithm. The proposed architectures help in optimizing the hardware for power that dissipates. The technique of clock gating helps in reducing power and reduces the computation time in real time processing. This proposed design achieved the power reduction using the clock gating technique and reduces the power for around 31.3% compared to the actual circuit.

REFERENCES

[1]. Abdulghani, Ahmadshahrizan & MatIsa, NorAshidi. (2014). "Underwater image quality enhancement through composition of dual-intensity images and Rayleigh-stretching". SpringerPlus.3. 757. 10.1186/2193-1801-3- 757.

[2]. C. O. Ancuti, C. Ancuti, C. De Vleeschouwer and P. Bekaert, "Color Balance and Fusion for Underwater Image Enhancement," in IEEE Transactions on Image Processing, vol. 27, no. 1, pp. 379-393, Jan. 2018, doi: 10.1109/TIP.2017.2759252.

[3]. "IEEE Standard for Floating-Point Arithmetic," in IEEE Std 754-2019 (Revision ofIEEE754-2008),vol.,no.,pp.1-84,22July 2019, doi:10.1109/IEEESTD.2019.8766229.

[4]. Patel, Sagar& Patel, Krinesh& Patel, Keval& Patel, Chaitanya. (2019). "Image Enhancement on FPGA using Verilog" in International Journal of Technical Innovation in Modern Engineering &Science (IJTIMES) Impact Factor: 5.22 (SJIF-2017), e-ISSN: 2455-2585 Volume 5, Issue 03, March-2019.

[5]. Dakre, Kalyani A. and P. N. Pusdekar. "A Review on Image Enhancement using Hardware co-simulation for Biomedical Application" (2015) in International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Volume 3 Issue 12,pp.4438-4441.

[6]. Chiuchisan, I., Cerlinca, M., &Potorac, A.D. "Image Enhancement Methods Approach usingVerilogHardwareDescriptionLanguage"in 11th International Conference on DEVELOPMENT AND APPLICATIONSYSTEMS, Suceave, Romania, May 17-19, pp.145-148,2012.

[7]. C. O. Ancuti, C. Ancuti, C. De Vleeschouwer and P. Bekaert, "Color Balance and Fusionfor Underwater Image Enhancement," in IEEE Transactions on Image Processing, vol. 27, no. 1, pp. 379-393, Jan. 2018, doi: 10.1109/TIP.2017.2759252.

[8]. "IEEE Standard for Floating-Point Arithmetic," in IEEE Std 754-2019 (Revision ofIEEE754-2008),vol.,no.,pp.1-84,22July 2019, doi:10.1109/IEEESTD.2019.8766229.

[9]. Patel, Sagar& Patel, Krinesh& Patel, Keval& Patel, Chaitanya. (2019). "Image Enhancement on FPGA using Verilog" in International Journal of Technical Innovation in Modern Engineering &Science (IJTIMES) Impact Factor: 5.22 (SJIF-2017), e-ISSN: 2455-2585 Volume 5, Issue 03, March-2019.

[10]. Dakre, Kalyani A. and P. N. Pusdekar. "A Review on Image Enhancement using Hardware co-simulation for Biomedical Application" (2015) in International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Volume 3 Issue 12,pp.4438-4441.

[11]. Chiuchisan, I., Cerlinca, M., &Potorac, A.D. "Image Enhancement Methods Approach usingVerilogHardwareDescriptionLanguage"in11th International Conference on DEVELOPMENT AND APPLICATIONSYSTEMS, Suceave, Romania, May 17-19, pp.145-148,2012.

[12]. Rohit Pravin Mungekar, R. Jayagowwri, "A Hardware Design of Red Channel Compensation Unit for Underwater Image Processing"' Journal of Chengdu University of Technology , Volume 26, Issue.7, 2021 .

[13]. Keshava Koushik.S R. Jayagowri, Karthik.S.Rao, Karthik.C.V, "Design and Implementation of Low-Power Pipelined FFT Processor", International Journal of VLSI & Signal Processing Applications, Volume2, Issue4,PP-330-335.